Mingjie Lin

Department of Electrical Engineering & Computer Science
HEC Building, Room 237
Orlando, FL 32816

(O) 407-882-2298
http://www.eecs.ucf.edu/∼mingjie

Education/Work

- **University of Central Florida** — Orlando, FL
  Associate Professor, EECS — *January 2017 - Now*
- **University of Central Florida** — Orlando, FL
  Assistant Professor, EECS — *January 2011 - 2017*
- **UC Berkeley** — Berkeley, CA
  Post-Doctoral Scholar, EECS — *March 2009 - August 2010*
- **Tabula Inc.** — Sunnyvale, CA
  Senior Engineer — *June 2008 - March 2009*
- **Stanford University** — Stanford, CA
  Ph. D., Electrical Engineering — *September 2001 - 2008*

Research Interests

Areas—Integrated Circuit and System Design, Reconfigurable Computing, and Computer Architecture.

Themes—My research focuses on developing alternative, non-Boolean, non-CMOS computing paradigms capable of penetrating the digital CMOS computational efficiency barrier posed by quantum-related device physics. Specifically, we investigate how to transcend deterministic computing by natively exploiting randomness-driven physical phenomenon, either from CMOS devices under extreme conditions or from emerging spin-torque devices, to effectively compute.

Awards and Honors

1. **UCF Reach for the Stars (1 of 5 recipients)**, 2017.
2. **CECS Dean's Advisory Board Faculty Fellow, UCF**, 2017.
3. **NSF CAREER award, CISE-SHF**, 2016.
4. **UCF Teaching Incentive Program (TIP) Award**, 2016
5. **AFOSR: Summer Faculty Fellowship Award (USAF-SFFP)**, 2016
6. **SAIC Faculty Fellow**, 2014

Selected Publications

Note: ⋆ denotes the corresponding author. † denotes the student author from Dr. Lin's research group.

Journal Papers

1. Mohammed Alawad† and **M. Lin⋆**; "*Memory-Efficient Probabilistic 2-D Finite Impulse Response (FIR) Filter*", Page(s): 69 - 82, Volume: 4, Issue: 1, IEEE Transactions on Multi-Scale Computing Systems, 2018.
2. Yu Bai†, Ronald F. DeMara, Jia Di, and **M. Lin⋆**; "*Clockless Spintronic Logic: A Robust and Ultra-Low Power Computing Paradigm*", IEEE Transactions on Computers, Vol. 67, Issue 5, Page 631-645, 2018.

3. Yu Bai†, Deliang Fan, and **M. Lin⋆**; "*Stochastic-Based Synapse and Soft-Limiting Neuron with Spintronic Devices for Low Power and Robust Artificial Neural Networks*", Accepted and to be printed in the IEEE Transactions on Multi-Scale Computing Systems, 2018.

4. Mohammed Alawad†, Yu Bai†, and **M. Lin⋆**; "*Boosting Computing Performance of Embedded Applications with Irregular Stride Memory Access Patterns via Hardware-Assisted Dynamic Graph*", Accepted and to be printed in Journal of Low Power Electronics and Applications, 2017.

5. Mohammed Alawad† and **M. Lin⋆**; "*Sketching Computation with Stochastic Processing Engines*", ACM Journal on Emerging Technologies in Computing Systems (JETC) - Special Issue on Hardware and Algorithms for Learning On-a-chip and Special Issue on Alternative Computing Systems, Volume 13 Issue 3, May 2017. Article No. 46.

6. Mohammed Alawad†, Yu Bai†, Ronald DeMara, and **M. Lin⋆**; "*Robust Large-Scale Convolution through Stochastic-Based Processing without Multipliers*", IEEE Transactions on Emerging Topics in Computing, 2017.

7. Mohammed Alawad† and **M. Lin⋆**; "*Stochastic-Based Deep Convolutional Networks with Reconfigurable Logic Fabric*", Page(s): 242 - 256, Volume: 2, Issue: 4, IEEE Transactions on Multi-Scale Computing Systems, 2016.

8. Mohammed Alawad† and **M. Lin⋆**; "*Survey on Stochastic-based Computing Paradigms*", IEEE Transactions on Emerging Topics in Computing, 2016.

9. Yu Bai† and **Mingjie Lin⋆**. "*Stochastic-Based Spin-Programmable Gate Array with Emerging MTJ Device Technology*". Journal of Low Power Electronics and Applications. 2016, 6(3), 15; doi:10.3390/jlpea6030015.

10. **M. Lin⋆**, S. Chen, R. DeMara, and J. Wawrzynek; "*ASTRO: Synthesizing application-specific reconfigurable hardware traces to exploit memory-level parallelism*", Microprocessors and Microsystems, Vol. 10, No. 5, Pages 10-22, March 26, 2015, DOI:10.1016/j.micpro.2015.03.005.

11. Mohammed Alawad†, Ronald F. DeMara, **Mingjie Lin⋆**. "*Stochastically Estimating Modular Criticality in Large-Scale Logic Circuits Using Sparsity Regularization and Compressive Sensing*". Journal of Low Power Electronics and Applications. vol. 5, no. 1, pp. 3-37, April 27, 2015. http://www.mdpi.com/2079-9268/5/1/3/pdf.

12. Yu Bai†, Mohammed Alawad†, Ronald F. DeMara, **Mingjie Lin⋆**. "*Optimally Fortifying Logic Reliability through Criticality Ranking*". Electronics. vol. 4, no. 1, pp. 150-172, March 18. 2015. http://www.mdpi.com/2079-9292/4/1/150/pdf

13. N. Imran, J. Lee, Y. Kim, **M. Lin**, and R. F. DeMara⋆; "*Amorphous Slack Methodology for Autonomous Fault-Handling in Reconfigurable Devices*", International Journal of Multimedia and Ubiquitous Engineering (IJMUE), Vol. 7, No. 4, Pages 29-44, October, 2012.

14. **Mingjie Lin⋆**, Yu Bai†, and John Wawrzynek; "*Selectively Fortifying Reconfigurable Computing Device to Achieve Higher Error Resilience*", Journal of Electrical and Computer Engineering, vol.10, October, 2012.

15. Ilia Lebedev, Christopher Fletcher, Shaoyi Cheng, James Martin, Austin Doupnik, Daniel Burke, **Mingjie Lin**, and John Wawrzynek⋆; "*Exploring Many-core Design Templates for FPGAs and ASICs*"; International Journal of Reconfigurable Computing (IJRC), July 15. 2011. (Invited Paper).

16. **Mingjie Lin⋆** and John Wawrzynek, "*Improving Placements in FPGA with Dynamically Adaptive Stochastic Tunneling* ", in IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems, Volume 29, Issue 12, Pages 1858 - 1869, December, 2010.

17. **Mingjie Lin** and Abbas El Gamal⋆, "*Exploring FPGA Routing Architecture Stochastically* ", in IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems, Volume 29, Issue 10, Pages 1509 - 1522, September 20, 2010.

18. **Mingjie Lin** and Abbas El Gamal⋆, "*A Low-Power Field-Programmable Gate Array Routing Fabric*", Very Large Scale Integration (VLSI) Systems, IEEE Transactions on , vol.17, no.10, pp.1481-1494, Oct. 2009.

19. **Mingjie Lin**, Abbas El Gamal, Yi-chang Lu, and Simon Wong⋆, "*Performance Benefits of Monolithically Stacked 3D-FPGA (invited)* ", in IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems, Volume 26, Issue 2, February, 2007.

20. **Mingjie Lin** and Nick McKeown⋆, "*The Throughput of a Buffered Crossbar Switch* ", in IEEE Communications Letters, Volume 9, Issue 5, Page(s):465 - 467, May, 2005.

21. **Mingjie Lin** and Ting Wang, "*A Novel 3-D Transient Liquid Crystal Method for Numerical Fluid Dynamics Computation* ", in International Journal of Heat and Mass Transfer, Volume 45, Issue 17, Pages 3491-3501, August 2002.

Conference Papers

1. Y. Zou and **M. Lin⋆**. "*Very Large-Scale and Node-Heavy Graph Analytics with Heterogeneous FPGA+CPU Computing Platform* ". In Proceedings of the 2018 IEEE Computer Society Annual Symposium on VLSI (ISVLSI). Pages: 713 - 718, 2018.

2. Sayyed Jaffar Ali Raza and **M. Lin⋆**. "*Bio-Inspired Hyper-Redundant Robotic Arm Control with Hierarchical Deep Reinforcement Learning* ". In Proceedings of the 15th International Conference on Ubiquitous Robots (Accepted and TBP).

3. Shaahin Angizi, Zhezhi He, Yu Bai, Jie Han, **Mingjie Lin⋆**, and Deliang Fan. "*Leveraging Spintronic Devices for Efficient Approximate Logic and Stochastic Neural Network* ". In Proceedings of the 2018 ACM Great Lakes Symposium on VLSI (GLSVLSI), Chicago, IL, USA, May 23-25, 2018 (invited).

4. Juan Escobedo† and **Mingjie Lin⋆**. "*Parallelizing Non-Stencil Memory Accesses Through Coloring Weighted Conflict Graphs* ". In Proceedings of the 2018 Design Automation Conference (DAC18). (Full Paper) ACM, San Francisco, CA, USA.

5. Juan Escobedo† and **Mingjie Lin⋆**. "*Graph-Theoretically Optimal Memory Banking for Stencil-Based Computing Kernels*". In Proceedings of the 2018 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA 18). (Full Paper) ACM, Monterey, CA, USA.

6. Stephen Williams† and **Mingjie Lin⋆**. "*Architecture and Circuit Design of An All-Spintronic FPGA Device*". In Proceedings of the 2018 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA 18). (Full Paper) ACM, Monterey, CA, USA.

7. Juan Escobedo† and **M. Lin⋆**. "*Tessellating Memory Space for Parallel Access*". In Proceedings of the 22nd Asia and South Pacific Design Automation Conference (ASP-DAC 2017). Page 75-80, 2017.

8. Y. Bai†, H. Bo, W. Kuang, and **M. Lin⋆**. "*Magnetic domain wall implemented null convention logic*". In Proceedings of the 26rd ACM international conference on Great lakes symposium on VLSI (GLSVLSI2016).

9. Juan Escobedo† and **M. Lin⋆**. "*Tessellation-Based Multi-Block Memory Mapping Scheme for High-Level Synthesis with FPGA*". In Proceedings of The 2016 International Conference on Field-Programmable Technology (FPT '16). Page 125-132, 2016.

10. Y. Bai†, H. Bo, W. Kuang, and **M. Lin⋆**. "*Ultra-robust null convention logic circuit with emerging domain wall devices*". In Proceedings of the 2016 International Great Lakes Symposium on VLSI (GLSVLSI), Boston, MA, 2016, pp. 251-256. doi: 10.1145/2902961.2903019

11. M. Alawad and **M. Lin⋆**. "*Stochastic-Based Convolutional Networks with Reconfigurable Logic Fabric* ". In Proceedings of the 2016 IEEE Computer Society Annual Symposium on VLSI (ISVLSI). Pages: 713 - 718, 2016.

12. Faris S. Alghareb, **M. Lin⋆**, and Ronald F. DeMara "*Soft Error Effect Tolerant Temporal Self-Voting Checkers: Energy vs. Resilience Tradeoffs* ". In Proceedings of the 2016 IEEE Computer Society Annual Symposium on VLSI (ISVLSI). Pages: 571 - 576, 2016.

13. M. Alawad, A. Honardoost, M. Riera, and **M. Lin⋆**. "*Spin-Based Arbitrary Random Number Distributions using Magnetic Tunnel Junction*". In the Proceedings of 2016 IEEE Southeast Conference. Norfolk, VA. 30 March- 03 April, 2016.

14. Yu Bai, Yuchuan Sun, and **M. Lin⋆**. "*Stochastic-based logic circuit synthesis and implementation through large-fanin threshold logic with magnetic tunneling junctions*". 2016 International Conference on Integrated Circuits and Microsystems (ICICM) Pages: 55 - 60, 2016.

15. Y. Bai† and **M. Lin⋆**. "*Stochastic-based spin-programmable gate array with emerging MTJ device technology*". In Proceedings of the 2016 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA 16). (Poster) ACM, New York, NY, USA.

16. Y. Bai†, and **M. Lin⋆**. "*Universal Random Number Generation with Field-Programmable Analog Array and Magnetic Tunneling Junction (MTJ) Devices*". 14th IEEE International Conference on Ubiquitous Computing and Communications (IUCC-2015) to be held in Liverpool, England, UK, 26-28 October 2015.

17. A. Fuentes-Rivera†, **M. Lin⋆**, and H. M. Lugo-Cordero. "*Gabor Filter Approximation Based on New Evolutionary Stochastic PSO and DE techniques*". In Proceedings of the Milcom 2015 Track 1 - Waveforms and Signal Processing. Tampa, USA. 2015.

18. Mohammed Alawad†, Sinan Ismail, and **Mingjie Lin⋆**. "*Neural Network-Based Fuzzy Control Surface Implementation*". In the Proceedings of the third IEEE Global Conference on Signal and Information Processing (GlobalSIP). Orlando, FL, USA. 2015.

19. R. A. Ashraf, A. Al-Zahrani, N. Khoshavi, R. Zand, S. Salehi, A. Roohi, **M. Lin**, and R. F. DeMara⋆, "*Reactive Rejuvenation of CMOS Logic Paths using Self-Activating Voltage Domains*", in Proceedings of IEEE International Symposium on Circuits and Systems (ISCAS-2015), Lisbon, Portugal, May 24 - 27, 2015.

20. Mohammed Alawad†, and **Mingjie Lin⋆**. "*Energy-efficient imprecise reconfigurable computing through probabilistic domain transformation*". In Proceedings of the 2014 IEEE Dallas Circuits and Systems Conference (DCAS 2014). IEEE, Dallas, TX, USA, 1-4., Oct. 2014. DOI: 10.1109/DCAS.2014.6965329

21. Mohammed Alawad†, and **Mingjie Lin⋆**. "*FIR Filter Based on Stochastic Computing with Reconfigurable Digital Fabric*". In the Proceedings of the 23rd IEEE International Symposium on Field-Programmable Custom Computing Machines (FCCM 2015). IEEE, Vancouver, British Columbia, Canada., May 2015.

22. Mohammed Alawad†, and **Mingjie Lin⋆**. "*Quality-Scalable Signal Processing via Probabilistic Computing*". In the Proceedings of the The Sixth International Symposium on Highly Efficient Accelerators and Reconfigurable Technologies (HEART2015). Boston, MA, USA. June 2015.

23. Yu Bai† and **Mingjie Lin⋆**, "*Energy-Efficient Discrete Signal Processing with Field Programmable Analog Arrays (FPAAs)*". In Proceedings of the 2015 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA '15). ACM, New York, NY, USA, 84-93. DOI=10.1145/2684746.2689078, March 2015. http://doi.acm.org/10.1145/2684746.2689078

24. Mohammed Alawad† and **Mingjie Lin⋆**, "*Energy-Efficient High-Order FIR Filtering through Reconfigurable Stochastic Processing*", In Proceedings of the 2015 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA '15). ACM, New York, NY, USA, 95. DOI=10.1145/2684746.2689129, March 2015. http://doi.acm.org/10.1145/2684746.2689129

25. Yu Bai† and **Mingjie Lin⋆**, "*Stochastically computing discrete Fourier transform with reconfigurable digital fabric*", ReConFigurable Computing and FPGAs (ReConFig), 2014 International Conference on , vol., no., pp.1,7, 8-10 Dec. 2014. doi: 10.1109/ReConFig.2014.7032558

26. Mohammed Alawad† and **Mingjie Lin⋆**, "*Energy-efficient imprecise reconfigurable computing through probabilistic domain transformation* ". In Proceedings of the 2014 IEEE Dallas Circuits and Systems Conference (DCAS), Pages: 1 - 4, 2014.

27. Mohammed Alawad†, Yu Bai†, Ronald DeMara, and **Mingjie Lin⋆**. "*Energy-efficient multiplier-less discrete convolver through probabilistic domain transformation*". In Proceedings of the 2014 ACM/SIGDA international symposium on Field-programmable gate arrays (FPGA '14). ACM, New York, NY, USA, 185-188. Feb. 2014. DOI=10.1145/2554688.2554769 http://doi.acm.org/10.1145/2554688.2554769. (acceptance rate: 17.8%).

28. Yu Bai†, Mohammed Alawad†, and **Mingjie Lin⋆**. "*Optimally mitigating BTI-induced FPGA device aging with discriminative voltage scaling*" (abstract only). In Proceedings of the 2014 ACM/SIGDA international symposium on Field-programmable gate arrays (FPGA '14). ACM, New York, NY, USA, 246-246. Feb. 2014. DOI=10.1145/2554688.2554752 http://doi.acm.org/10.1145/2554688.2554752.

29. Mohammed Alawad†, Yu Bai†, and **Mingjie Lin⋆**, "*Probabilistic Domain Transformation: A Robust and Energy-Efficient Computing Means*" (regular paper), 2013 International Conference on Advanced Information Engineering and Education Science (ICAIEES 2013), Beijing, China, 256-261. Dec. 2015.

30. **Mingjie Lin⋆**, Shaoyi Cheng, and Wawrzynek, J., "*Extracting memory-level parallelism through reconfigurable hardware traces*", Reconfigurable Computing and FPGAs (ReConFig), 2013 International Conference on , vol., no., pp.1,8, 9-11 Dec. 2013 doi: 10.1109/ReConFig.2013.6732290 (acceptance rate: 27.1%).

31. Bai Yu†, Alawad, M.†, Riera, M.†, and **Mingjie Lin⋆**, "*Improving memory performance in reconfigurable computing architecture through hardware-assisted dynamic graph*", Reconfigurable Computing and FPGAs (ReConFig), 2013 International Conference on , vol., no., pp.1,8, 9-11 Dec. 2013 doi: 10.1109/ReConFig.2013.6732300. (acceptance rate: 27.1%).

32. Shaoyi Cheng, **Mingjie Lin**, Hao Jun Liu, Scott, S., and Wawrzynek, J.⋆, "Exploiting Memory-Level Parallelism in Reconfigurable Accelerators", Field-Programmable Custom Computing Machines (FCCM), 2012 IEEE 20th Annual International Symposium on , vol., no., pp.157,160, April 29 2012-May 1 2012 doi: 10.1109/FCCM.2012.35 (acceptance rate: 28%).

33. Naveed Imran, Jooheung Lee, Youngju Kim, **Mingjie Lin**, and Ronald F. DeMara⋆, "*Area-Efficient Fault-Handling for Survivable Signal-Processing Architectures*", International Conference on Advanced Signal Processing, Olympic Parktel, Seoul, Korea, March 30-31, 2012.

34. **Mingjie Lin**, Shaoyi Cheng, John Wawrzynek⋆, "*Using many-core architectural templates for FPGA-based computing*", (abstract only). the 2011 ACM/SIGDA International Symposium on Field Programmable Gate Arrays: 281. Feb. 2011.

35. **Mingjie Lin⋆**, Yu Bai†, John Wawrzynek; "*Discriminatively Fortified Computing with Reconfigurable Digital Fabric*", High-Assurance Systems Engineering (HASE), 2011 IEEE 13th International Symposium on , vol., no., pp.112-119, 10-12 Nov. 2011.

36. Ilia Lebedev, Shaoyi Cheng, Austin Doupnik, James Martin, Christopher Fletcher, Daniel Burke, **Mingjie Lin** and John Wawrzynek⋆, "*MARC: A Many-Core Approach to Reconfigurable Computing*", in Proceedings of the 2010 International Conference on Reconfigurable Computing and FPGAs (RECONFIG '10). IEEE Computer Society, Washington, DC, USA, 7-12. DOI=10.1109/ReConFig.2010.49 http://dx.doi.org/10.1109/ReConFig.2010.49

37. Mingjie Lin and John Wawrzynek⋆, "*Cascading Deep Pipelines to Achieve High Throughput in Numerical Reduction Operations*", in Proceedings of the 2010 International Conference on Reconfigurable Computing and FPGAs (RECONFIG '10). IEEE Computer Society, Washington, DC, USA, 103-108. DOI=10.1109/ReConFig.2010.70 http://dx.doi.org/10.1109/ReConFig.2010.70

38. **Mingjie Lin**, Ilia Lebedev, and John Wawrzynek⋆, "*OpenRCL: Low-Power High-Performance Computing with Reconfigurable Devices* ", Field Programmable Logic and Applications (FPL), 2010 International Conference on , vol., no., pp.458,463, Aug. 31 2010-Sept. 2 2010 doi: 10.1109/FPL.2010.93

39. **Mingjie Lin**, Ilia Lebedev, and John Wawrzynek⋆, "*High-Throughput Bayesian Computing Machine with Reconfigurable Hardware* ", in Proceedings of the 18th annual ACM/SIGDA international symposium on Field programmable gate arrays (FPGA '10). ACM, New York, NY, USA, 73-82. DOI=10.1145/1723112.1723127 http://doi.acm.org/10.1145/1723112.1723127

40. **Mingjie Lin⋆**, David McCluskey, and Yaling Ma, "*Scalable Architecture for Programmable Quantum Gate Array* ", (abstract), in Proceedings of the 18th annual ACM/SIGDA international symposium on Field programmable gate arrays (FPGA '10). ACM, New York, NY, USA, 290-290. DOI=10.1145/1723112.1723182 http://doi.acm.org/10.1145/1723112.1723182

41. **Mingjie Lin⋆** and Yaling Ma, "*Base-Calling in DNA Pyrosequencing with Reconfigurable Bayesian Network* ", in Proceedings of the 2009 International Conference on Reconfigurable Computing and FPGAs (RECONFIG '09). IEEE Computer Society, Washington, DC, USA, 95-100. DOI=10.1109/ReConFig.2009.79 http://dx.doi.org/10.1109/ReConFig.2009.79

42. **Mingjie Lin** and Abbas El Gamal⋆, "*TORCH: A Tool for Segmented Routing Channel Design in FPGAs* ", in Proceedings of the 16th international ACM/SIGDA symposium on Field programmable gate arrays (FPGA '08). ACM, New York, NY, USA, 131-138. DOI=10.1145/1344671.1344693 http://doi.acm.org/10.1145/1344671.1344693

43. **Mingjie Lin⋆**, "*The Amorphous FPGA Architecture* ", in Proceedings of the 16th international ACM/SIGDA symposium on Field programmable gate arrays (FPGA '08). ACM, New York, NY, USA, 191-200. DOI=10.1145/1344671.1344700 http://doi.acm.org/10.1145/1344671.1344700

44. **Mingjie Lin⋆**, Steve Ferguson, Yaling Ma, and Timothy Greene, "*HAFT: a Hybrid FPGA with Amorphous and Fault-Tolerant Architecture* ". Circuits and Systems, 2008. ISCAS 2008. IEEE International Symposium on , vol., no., pp.1348,1351, 18-21 May 2008 doi: 10.1109/ISCAS.2008.4541676

45. **Mingjie Lin⋆**, Jianying Luo, and Yaling Ma, "*A low-power monolithically stacked 3D-TCAM*", Circuits and Systems, 2008. ISCAS 2008. IEEE International Symposium on , vol., no., pp.3318,3321, 18-21 May 2008 doi: 10.1109/ISCAS.2008.4542168

46. **Mingjie Lin** and Abbas El Gamal⋆, "*A Routing Fabric for Monolithically Stacked 3D-FPGA* ", in Proceedings of the 2007 ACM/SIGDA 15th international symposium on Field programmable gate arrays (FPGA '07). ACM, New York, NY, USA, 3-12. Feb. 2007. DOI=10.1145/1216919.1216921 http://doi.acm.org/10.1145/1216919.1216921

47. **Mingjie Lin⋆** and Yaling Ma, "*Collaborative Routing Architecture for FPGA* ". Circuits and Systems, 2007. ISCAS 2007. IEEE International Symposium on , vol., no., pp.3700,3703, 27-30 May 2007 doi: 10.1109/ISCAS.2007.378646

48. **Mingjie Lin**, Abbas El Gamal, Yi-chang Lu, and Simon Wong⋆, "*Performance Benefits of Monolithically Stacked 3D-FPGA* ", in Proceedings of the 2006 ACM/SIGDA 14th international symposium on Field programmable gate arrays (FPGA '06). ACM, New York, NY, USA, 113-122. Feb. 2006. DOI=10.1145/1117201.1117219 http://doi.acm.org/10.1145/1117201.1117219

49. **Mingjie Lin⋆** and Yashar Ganjali, "*Energy-efficient Rate Scheduling in Wireless Links using Computational Geometric Algorithms* ", in proceedings of the International Wireless Communications and Mobile Computing Conference (IWCMC), Vancouver, Canada, July 2006.

50. **Mingjie Lin⋆** and Yaling Ma, "*k-Server Optimal Task Scheduling Problem with Convex Cost Function* ", Modeling and Optimization in Mobile, Ad Hoc, and Wireless Networks, 2005. WIOPT 2005. Third International Symposium on , vol., no., pp.345,350, 3-7 April 2005 doi: 10.1109/WIOPT.2005.25

Current Contract or Grant Activities

1. **Hardware-Assisted Research Platform for Topographical Robotic Control with Infinity DOF**. Amount: $194,162.00. Share: 100%. PI. DoD DURIP from the Office of Naval Research. 2017.

2. **University Professor Engagement: Scouting Area of Artificial Intelligence and Deep Learning**. Amount: $25,000.00. Share: 100%. PI. Siemens Energy, Inc.. 2017.

3. **CAREER: iMPACT: Metaphysical and Probabilistic-Based Computing Transformation with Emerging Spin-Transfer Torque Device Technology**. Amount: $541,321.00. Share: 100%. PI. NSF SHF. 2016.

4. **Bio-Inspired Logic Design with Graph and Field Theory**. Amount: $271,642.20. Share: 100%. PI. NSF SHF. 2013.

5. **Minimum-Energy Bio-Inspired Analogic Computing Devices with Stochastic Switching Transistors under Ultra-Low VDD**. Amount: $148,416.00. Share: 100%. PI. NSF BRIGE. 2013.

6. **Hardware-Assisted Large-Scale Neuroevolution for Multiagent Learning**. Amount: $201,500.00. Share: 49%. PI. DoD DURIP. 2012.

7. **Discriminatively Fortified Computing for Integrated Circuit (IC) Devices**. Amount: $7,500.00. Share: 100%. PI. UCF. 2011.

8. **Collaborative Research: Florida-IT-Pathways to Success (Flit-Path)** . Amount: $1,526,600.00. Share: 6%. Co-PI. NSF. 2016.

9. **Multi-functional Integrated System Technology Center (an NSF I/UCRC)**. Amount: $1,000. Share: 2%. UCF Faculty Member. NSF. 2015.

10. **REU Site: Research Experiences in the Internet of Things (IoT)** Amount: $12,675. Share: 5%. co-PI. NSF. 2015.